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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/010,569 | 11/13/2001 | Brian C. Barnes | 2000.056600/TT4086 | 4325 |

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| EXAMINER | |
|---|---|
| INOA, MIDYS | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2188 | 8 |

DATE MAILED: 05/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/010,569 | BARNES ET AL. | |
| | Examiner | Art Unit | |
| | Midys Inoa | 2188 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim1-9, 11-19, 21, 23-25, 27-34 and 36-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Maruyama (6,052,763).

Regarding Claims 1, 8, 11-13, 23, 32 and 36, Maruyama teaches a Processing Unit 340 ("execution unit") coupled to the memory unit 10 through the use of bus 15 and a memory controller 20 ("memory management unit") coupled to the DRAM memory 19. Maruyama also discloses a system bus interface unit 16, a comparator 23 and a register unit 21 ("security check unit") in which the register 21 receives an access address ("physical address"), which refers to an access point within DRAM memory 19, and thus must reside within a memory page in DRAM memory 19 (Figure 4). Using the access address, the system bus interface unit determines an identification of the bus mater (master ID) and sends it to comparator 23 through register 22 ("use the physical address to ...obtain a security attribute of the selected memory page", Column 5, lines 19-40). Using a bus master ID table ("security attribute data structure") as an identifier, the comparator 23 compares information from the master ID table (comparator and master ID table cooperate to determine if a processor is a requester with privileges, Column 6, lines 29-32) to the processor's master ID ("security attribute"), supplied by the bus interface unit through register 22, to determine if the requesting processor is a bus master with privileges

for performing a transaction. If the processor's master ID does not match, the comparator outputs a signal indicating an error ("fault signal"); if there is a match, ad different signal is outputted (Column 6, lines 11-40, Column 5, lines 20-40). In this case, the processor master ID represents a security attribute since the system uses it to ensure that the processor trying to access the memory is permitted to do so. **Although comparator 23 does not directly compare values from the master ID table with the processor's master ID, it does compare the information temporarily stored in register 22 with the processor's master ID. Since the information stored in register 22 comes from the master ID table, the comparator 23 indirectly compares information from the master ID table with the processor's master ID.**

Regarding Claims 2, 14, 21, 24 and 29, Maruyama teaches a master ID data structure 24 comprising a master ID table ("table directory") and a lookup table ("security attribute table", Column 6, lines 48-54).

Regarding Claims 3-6, 15-18, 27-28, 30-31, and 37, Maruyama teaches using a master ID table ("accessing one security attribute data structure") to extract a master ID ("obtain additional security attribute", "SCID") and compare it to the master ID of the accessing processor. The master IDs in question are indicators of the security level of the accessing processor since they determine if the processor is authorized to perform any transactions in the memory system (Column 6, lines 30-55, Figure 4).

Regarding Claim 7, Maruyama teaches a comparator ("security check logic") obtaining a master ID ("security attribute") for the accessing processor from a master ID table ("security attribute structure") in order to compare the processor's master ID with the stored master ID (see Figure 4, Column 6 lines 29-40).

Regarding Claims 9, 19, 25 and 33, Maruyama teaches producing an output signal dependent on the comparison of the master ID from the master ID table and the master ID from the requesting processor. The result of such comparison determines what the privileges of the processor are and whether it is authorized to perform any transactions in the memory system ("security attributes").

Regarding Claim 34, Maruyama teaches a using an access address to obtain the master ID ("security attribute") for an accessing processor wherein a master ID data structure 24 comprises a master ID table ("table directory") and a lookup table ("security attribute table", Column 6, lines 48-54).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim10, 20, 22, 26, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama (6,052,763) in vie of applicant's admitted prior art.

Regarding Claims 10, 22, 26, and 35, Maruyama teaches the memory management system of claims 1, 13, and 23. Maruyama does not teach security attributes comprising a user/supervisor (U/S) bit and a read/write (R/W) bit. Applicant's admitted prior art discloses the memory protection features of an user/supervisor (U/S) bit and a read/write (R/W) bit where U/S=0 indicates that the memory page is an operating system page, U/S=1 indicates that the

memory page is an user memory page, R/W=0 indicates that only read accesses are allowed, and R/W=1 indicates that both read and write accesses are allowed to the memory page (Page 4, lines 4-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the protection features disclosed in applicant's admitted prior art to the memory management system of Maruyama since these features would add further security to the system by allowing the further access controls such as user or supervisor assigned memory areas and memory areas assigned as read-only or read-write areas.

Regarding Claim 20, Maruyama teaches the memory management system of claim 13. Maruyama does not teach a physical address within a selected memory page including a base address and an offset. Applicant's admitted prior art teaches a lower portion of an address ("offset") being used as an index of the memory page and a page frame base address being used to select the corresponding memory page. When the offset and the base address are combined, they form a physical address (Page 3, lines 21-25). It would have been obvious to one of ordinary skill in the art at the time the invention was made to give the system the ability to produce a physical address from the input of a linear address since such ability would allow the system in the case where linear addresses are being inputted.

***Response to Arguments***

5. Applicant's arguments filed March 16th, 2004 have been fully considered but they are not persuasive.

Applicant argues that comparator 23 of Maruyama (6,052,763) compares the temporarily stored bus master ID with the ID of the requesting device and does not compare the values from the master ID table to the bus master ID of the requesting device. **Although comparator 23**

**does not directly compare values from the master ID table with the processor's master ID, it does compare the information temporarily stored in register 22 with the processor's master ID. Since the information stored in register 22 comes from the master ID table, the comparator 23 indirectly compares information from the master ID table with the processor's master ID.**

*Conclusion*

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (703) 305-7850. The examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Midys Inoa
Examiner
Art Unit 2188

MI

5/27/04

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER